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POWER ELECTRONICS HANDBOOK

DEVICES, CIRCUITS, AND APPLICATIONS

Third Edition

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The Power Diode

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2.1 Diode as a Switch

Among all the static switching devices used in power electronics (PE), the power diode is perhaps the simplest. Its circuit symbol is shown in Fig. 2.1. It is a two terminal device, and terminal A is known as the anode whereas terminal K is known as the cathode. If terminal A experiences a higher potential compared to terminal K, the device is said to be forward biased and a current called forward current (I_F) will flow through the device in the direction as shown. This causes a small voltage drop across the device (<1 V), which in ideal condition is usually ignored. On the contrary, when a diode is reverse biased, it does not conduct and a practical diode do experience a small current flowing in the reverse direction called the leakage current. Both the forward voltage drop and the leakage current are ignored in an ideal diode. Usually in PE applications a diode is considered to be an ideal static switch.

The characteristics of a practical diode show a departure from the ideals of zero forward and infinite reverse impedance, as shown in Fig. 2.2a. In the forward direction, a potential barrier associated with the distribution of charges in the vicinity of the junction, together with other effects, leads to a voltage drop. This, in the case of silicon, is in the range of 1 V for currents in the normal range. In reverse, within the normal operating range of voltage, a very small current flows which is largely independent of the voltage. For practical purposes, the static characteristics is often represented by Fig. 2.2b. In the figure, the forward characteristic is expressed as a threshold voltage V_o and a linear incremental or slope resistance, r. The reverse characteristic remains the same over the range of possible leakage currents irrespective of voltage within the normal working range.

2.2 Properties of PN Junction

From the forward and reverse biased condition characteristics, one can notice that when the diode is forward biased, current rises rapidly as the voltage is increased. Current in the reverse biased region is significantly small until the breakdown voltage of the diode is reached. Once the applied voltage is over this limit, the current will increase rapidly to a very high value limited only by an external resistance.

DC diode parameters. The most important parameters are the followings:

- ***Forward voltage, V_F*** is the voltage drop of a diode across A and K at a defined current level when it is forward biased.
- ***Breakdown voltage, V_B*** is the voltage drop across the diode at a defined current level when it is beyond reverse biased level. This is popularly known as avalanche.
- ***Reverse current I_R*** is the current at a particular voltage, which is below the breakdown voltage.

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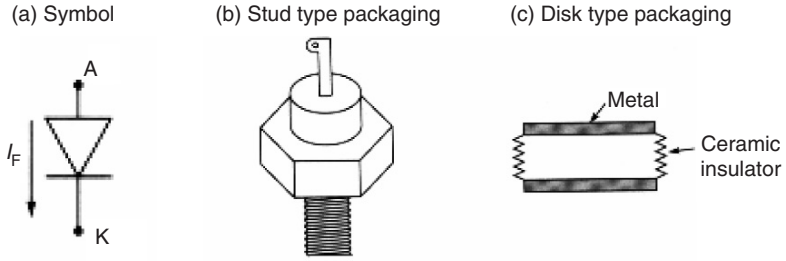

FIGURE 2.1 Power diode: (a) symbol; (b) and (c) types of packaging.

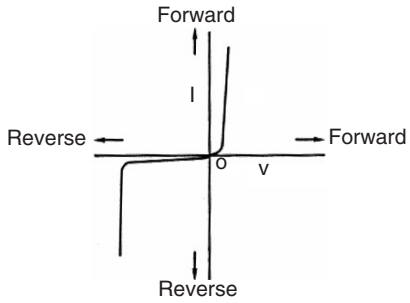

FIGURE 2.2a Typical static characteristic of a power diode (forward and reverse have different scale).

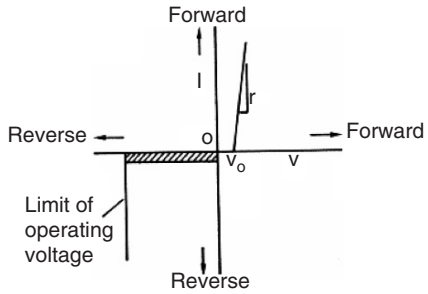

FIGURE 2.2b Practical representation of the static characteristic of a power diode.

AC diode parameters. The commonly used parameters are the followings:

- ***Forward recovery time, t_{FR}*** is the time required for the diode voltage to drop to a particular value after the forward current starts to flow.
- ***Reverse recovery time t_{rr}*** is the time interval between the application of reverse voltage and the reverse current dropped to a particular value as shown in Fig. 2.3. Parameter t_a is the interval between the zero crossing of the diode current to when it becomes I_{RR}. On the other hand, t_b is the time interval from the maximum reverse recovery current to approximately 0.25 of I_{RR}. The ratio of the two parameters t_a and t_b is known as the softness factor (SF). Diodes with abrupt recovery characteristics are used for high frequency switching.

In practice, a design engineer frequently needs to calculate the reverse recovery time. This is in order to evaluate the possibility of high frequency switching. As a thumb rule, the lower t_{RR} the faster the diode can be switched.

$$t_{rr} = t_a + t_b \tag{2.1}$$

If t_b is negligible compared to t_a which is a very common case, then the following expression is valid:

$$t_{RR} = \sqrt{\frac{2Q_{RR}}{(di/dt)}}$$

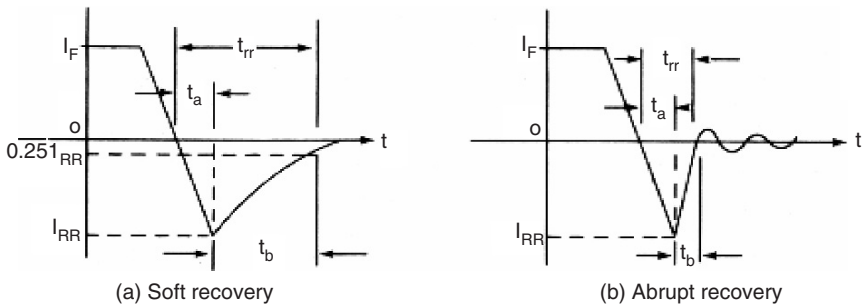

FIGURE 2.3 Diode reverse recovery with various softness factors.

from which the reverse recovery current

$$I_{RR} = \sqrt{\frac{di}{dt} 2Q_{RR}}$$

where Q_{RR} is the storage charge and can be calculated from the area enclosed by the path of the recovery current.

EXAMPLE 2.1 The manufacturer of a selected diode gives the rate of fall of the diode current $di/dt = 20\,\text{A}/\mu\text{s}$, and its reverse recovery time $t_{rr} = 5\,\mu\text{s}$. What value of peak reverse current do you expect?

SOLUTION. The peak reverse current is given as:

$$I_{RR} = \sqrt{\frac{di}{dt} 2Q_{RR}}$$

The storage charge Q_{RR} is calculated as:

$$Q_{RR} = \frac{1}{2}\frac{di}{dt} t_{rr}^2 = 1/2 \times 20\,\text{A}/\mu\text{s} \times (5 \times 10^{-6})^2 = 50\,\mu\text{C}$$

Hence,

$$I_{RR} = \sqrt{20\,\frac{\text{A}}{\mu\text{s}} \times 2 \times 50\,\mu\text{C}} = 44.72\,\text{A}$$

- ***Diode capacitance***, C_D is the net diode capacitance including the junction (C_J) plus package capacitance (C_P).

In high-frequency pulse switching, a parameter known as transient thermal resistance is of vital importance since it indicates the instantaneous junction temperature as a function of time under constant input power.

2.3 Common Diode Types

Depending on their applications, diodes can be segregated into the following major divisions:

Small signal diode: They are perhaps the most widely used semiconductor devices used in wide variety of applications. In general purpose applications, they are used as a switch in rectifiers, limiters, capacitors, and in wave-shaping. Some common diode parameters a designer needs to know are the forward voltage, reverse breakdown voltage, reverse leakage current, and the recovery time.

Silicon rectifier diode: These are the diodes, which have high forward current carrying capability, typically up to several hundred amperes. They usually have a forward resistance of only a fraction of an ohm while their reverse resistance is in the mega-ohm range. Their primary application is in power conversion, like in power supplies, UPS, rectifiers/inverters, etc. In case of current exceeding the rated value, their case temperature will rise. For stud-mounted diodes, their thermal resistance is between 0.1 and 1°C/W.

Zener diode: Its primary applications are in the voltage reference or regulation. However, its ability to maintain a certain voltage depends on its temperature coefficient and the impedance. The voltage reference or regulation applications of zener diodes are based on their avalanche properties. In the reverse biased mode, at a certain voltage the resistance of these devices may suddenly drop. This occurs at the zener voltage V_X, a parameter the designer knows beforehand.

Figure 2.4 shows a circuit using a zener diode to control a reference voltage of a linear power supply. Under normal operating condition, the transistor will transmit power to the load (output) circuit. The output power level will depend on the transistor base current. A very high base current will impose a large voltage across the zener and it may attain zener voltage V_X, when it will crush and limit the power supply to the load.

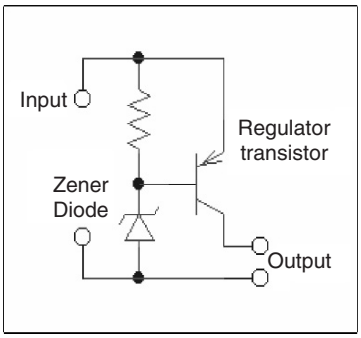

FIGURE 2.4 Voltage regulator with a zener diode for reference.

Photo diode: When a semiconductor junction is exposed to light, photons generate hole–electron pairs. When these charges diffuse across the junction, they produce photocurrent. Hence this device acts as a source of current, which increases with the intensity of light.

Light emitting diode (***LED***): Power diodes used in PE circuits are high power versions of the commonly used devices employed in analog and digital circuits. They are manufactured in wide varieties and ranges. The current rating can be from a few amperes to several hundreds while the voltage rating varies from tens of volts to several thousand volts.

2.4 Typical Diode Ratings

2.4.1 Voltage Ratings

For power diodes, a given datasheet has two voltage ratings. One is the repetitive peak inverse voltage (V_{RRM}), the other is the non-repetitive peak inverse voltage. The non-repetitive voltage (V_{RM}) is the diodes capability to block a reverse voltage that may occur occasionally due to a overvoltage surge.

Repetitive voltage on the other hand is applied on the diode in a sustained manner. To understand this, let us look at the circuit in Fig. 2.5.

EXAMPLE 2.2 Two equal source voltages of 220 V peak and phase shifted from each other by 180° are supplying a common load as shown. (a) Show the load voltage; (b) describe when diode D1 will experience V_{RRM}; and (c) determine the V_{RRM} magnitude considering a safety factor of 1.5.

SOLUTION. (a) The input voltage, load voltage, and the voltage across D1 when it is not conducting (V_{RRM}) are shown in Fig. 2.5b.

(b) Diode D1 will experience V_{RRM} when it is not conducting. This happens when the applied voltage $V1$ across it is in the negative region (from 70 to 80 ms as shown in the figure) and consequently the diode is reverse biased. The actual ideal voltage across it is the peak value of the two input voltages i.e. $220 \times 2 = 440$ V. This is because when D1 is not conducting, D2 conducts. Hence in addition V_{an}, V_{bn} is also applied across it since D2 is practically shorted.

(c) The $V_{RRM} = 440$ V is the value in ideal situation. In practice, higher voltages may occur due to stray circuit inductances and/or transients due to the reverse recovery of the diode. They are hard to estimate. Hence, a design engineer would always use a safety factor to cater to these overvoltages. Hence, one should use a diode with a $220 \times 2 \times 1.5 = 660$ V rating.

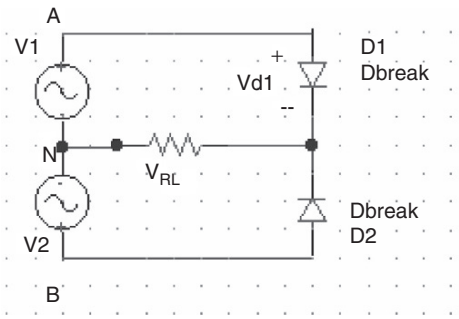

FIGURE 2.5a The circuit.

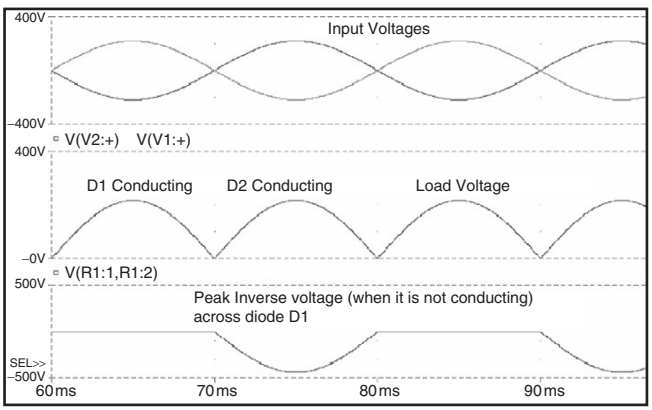

FIGURE 2.5b The waveforms.

2.4.2 Current Ratings

Power diodes are usually mounted on a heat sink. This effectively dissipates the heat arising due to continuous conduction. Hence, current ratings are estimated based on temperature rise considerations. The datasheet of a diode normally specifies three different current ratings. They are (1) the average current, (2) the rms current, and (3) the peak current. A design engineer must ensure that each of these values is not exceeded. To do that, the actual current (average, rms, and peak) in the circuit must be evaluated either by calculation, simulation, or measurement. These values must be checked against the ones given in the datasheet for that selected diode. The calculated values must be less than or equal to the datasheet values. The following example shows this technique.

EXAMPLE 2.3 The current waveform passing through a diode switch in a switch mode power supply application is shown in Fig. 2.6. Find the average, rms, and the peak current.

SOLUTION. The current pulse duration is shown to be 0.2 ms within a period of 1 ms and with a peak amplitude of 50 A. Hence the required currents are:

$$I_{average} = 50 \times \frac{0.2}{1} = 10\,\text{A}$$

$$I_{rms} = \sqrt{50^2 \times \frac{0.2}{1}} = 22.36\,\text{A}$$

$$I_{peak} = 50\,\text{A}$$

Sometimes, a surge current rating and its permissible duration is also given in a datasheet. For protection of diodes and other semiconductor devices, a fast acting fuse is required. These fuses are selected based on their I^2t rating which is normally specified in a datasheet for a selected diode.

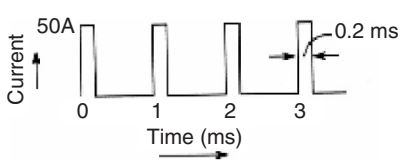

FIGURE 2.6 The current waveform.

2.5 Snubber Circuits for Diode

Snubber circuits are essential for diodes used in switching circuits. It can save a diode from overvoltage spikes, which may arise during the reverse recovery process. A very common snubber circuit for a power diode consists of a capacitor and a resistor connected in parallel with the diode as shown in Fig. 2.7.

When the reverse recovery current decreases, the capacitor by virtue of its property will try to hold the voltage across it, which, approximately, is the voltage across the diode. The resistor on the other hand will help to dissipate some of the energy stored in the inductor, which forms the I_{RR} loop. The dv/dt across a diode can be calculated as:

$$\frac{dv}{dt} = \frac{0.632 \times V_S}{\tau} = \frac{0.632 \times V_S}{R_S \times C_S} \tag{2.2}$$

where V_S is the voltage applied across the diode.

Usually the dv/dt rating of a diode is given in the manufacturers datasheet. Knowing dv/dt and the R_S, one can choose the value of the snubber capacitor C_S. The R_S can be calculated from the diode reverse recovery current:

$$R_S = \frac{V_S}{I_{RR}} \tag{2.3}$$

The designed dv/dt value must always be equal or lower than the dv/dt value found from the datasheet.

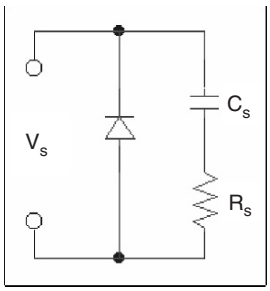

FIGURE 2.7 A typical snubber circuit.

2.6 Series and Parallel Connection of Power Diodes

For specific applications, when the voltage or current rating of a chosen diode is not enough to meet the designed rating, diodes can be connected in series or parallel. Connecting them in series will give the structure a high voltage rating that may be necessary for high-voltage applications. However, one must ensure that the diodes are properly matched especially in terms of their reverse recovery properties. Otherwise, during reverse recovery there may be a large voltage imbalances between the series connected diodes. Additionally, due to the differences in the reverse recovery times, some diodes may recover from the phenomenon earlier than the other causing them to bear the full reverse voltage. All these problems can effectively be overcome by connecting a bank of a capacitor and a resistor in parallel with each diode as shown in Fig. 2.8.

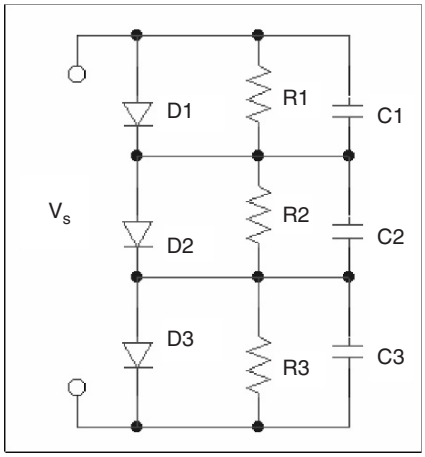

FIGURE 2.8 Series connected diodes with necessary protection.

If a selected diode cannot match the required current rating, one may connect several diodes in parallel. In order to ensure equal current sharing, the designer must choose diodes with the same forward voltage drop properties. It is also important to ensure that the diodes are mounted on similar heat sinks and are cooled (if necessary) equally. This will affect the temperatures of the individual diodes, which in turn may change the forward characteristics of diode.

Tutorial 2.1 Reverse Recovery and Overvoltages

Figure 2.9 shows a simple switch mode power supply. The switch (1-2) is closed at $t = 0$ s. When the switch is open, a freewheeling current $I_F = 20$ A flows through the load (RL), freewheeling diode (DF), and the large load circuit inductance (LL). The diode reverse recovery current is 20 A and it then decays to zero at the rate of 10 A/μs. The load is rated at 10 Ω and the forward on-state voltage drop is neglected.

(a) Draw the current waveform during the reverse recovery (I_{RR}) and find its time (t_{rr}).
(b) Calculate the maximum voltage across the diode during this process (I_{RR}).

SOLUTION. (a) A typical current waveform during reverse recovery process is shown in Fig. 2.10 for an ideal diode.

When the switch is closed, the steady-state current is, $I_{SS} = 200\,\text{V}/10\,\Omega = 20$ A, since under steady-state condition, the inductor is shorted. When the switch is open, the reverse recovery current flows in the right-hand side

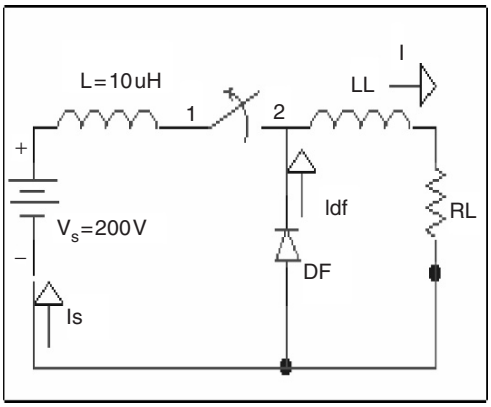

FIGURE 2.9 A simple switch mode power supply with freewheeling diode.

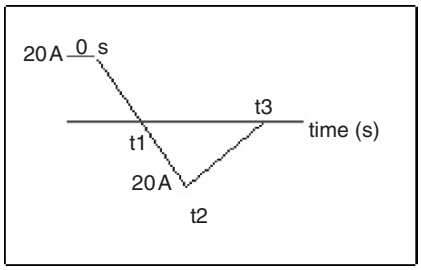

FIGURE 2.10 Current through the freewheeling diode during reverse recovery.

loop consisting of the LL, RL, and DF. The load inductance, LL is assumed to be shorted. Hence, when the switch is closed, the loop equation is:

$$V = L\frac{di_S}{dt}$$

from which

$$\frac{di_S}{dt} = \frac{V}{L} = \frac{200}{10} = 20\,\text{A}/\mu\text{s}$$

At the moment the switch is open, the same current keeps flowing in the right-hand side loop. Hence,

$$\frac{di_d}{dt} = -\frac{di_S}{dt} = -20\,\text{A}/\mu\text{s}$$

from time zero to time t_1 the current will decay at a rate of 20 A/s and will be zero at $t_1 = 20/20 = 1\,\mu$s. The reverse recovery current starts at this point and, according to the given condition, becomes 20 A at t_2. From this point on, the rate of change remains unchanged at 20 A/μs. Period $t_2 - t_1$ is found as:

$$t_2 - t_1 = \frac{20\,\text{A}}{20\,\text{A}/\mu\text{s}} = 1\,\mu\text{s}$$

From t_2 to t_3, the current decays to zero at the rate of 20 A/μs. The required time:

$$t_3 - t_2 = \frac{20\,\text{A}}{10\,\text{A}/\mu\text{s}} = 2\,\mu\text{s}$$

Hence the actual *reverse recovery time*: $t_{rr} = t_3 - t_1 = (1 + 1 + 2) - 1 = 3\,\mu$s.

(b) The diode experiences the maximum voltage just when the switch is open. This is because both the source voltage 200 V and the newly formed voltage due to the change in current through the inductor L. The voltage across the diode:

$$V_D = -V + L\frac{di_S}{dt} = -200 + (10\times10^{-6})(-20\times10^{6}) = -400\text{V}$$

Tutorial 2.2 Ideal Diode Operation, Mathematical Analysis, and PSPICE Simulation

This tutorial illustrates the operation of a diode circuit. Most of the PE applications operate at a relative high voltage, and in such cases, the voltage drop across the power diode usually is small. It is quite often justifiable to use the ideal diode model. An ideal diode has a zero conduction drop when it is forward biased and has zero current when it is reverse biased. The explanation and the analysis presented below is based on the ideal diode model.

Circuit Operation A circuit with a single diode and an RL load is shown in Fig. 2.11. The source V_S is an alternating sinusoidal source. If $V_S = \text{Esin}(\omega t)$, then V_S is positive when $0 < \omega t < \pi$, and V_S is negative when $\pi < \omega t < 2\pi$. When V_S starts becoming positive, the diode starts conducting and the positive source keeps the diode in conduction till ωt reaches π radians. At that instant, defined by $\omega t = \pi$ radians, the current through the circuit is not zero and there is some energy stored in the inductor. The voltage across an inductor is positive when the current through it is increasing and becomes negative when the current through it tends to fall. When the

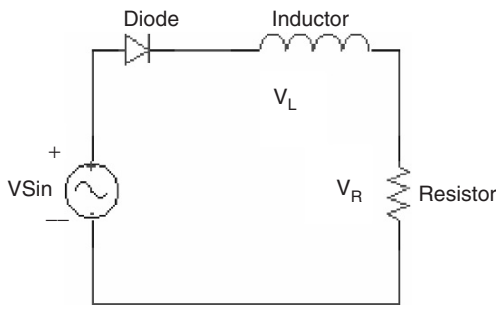

FIGURE 2.11 Circuit diagram.

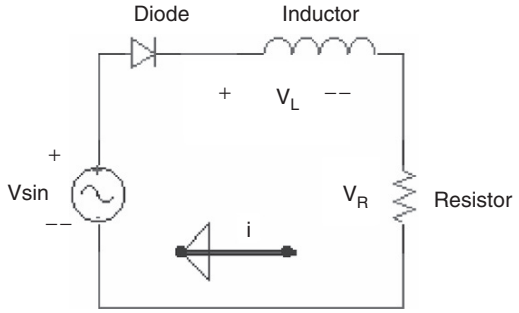

FIGURE 2.12 Current increasing, $0 < \omega t < \pi/2$.

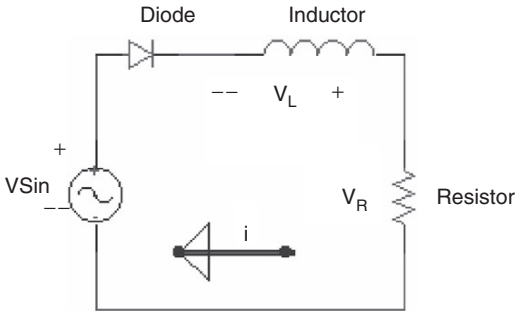

FIGURE 2.13 Current decreasing, $\pi/2 < \omega t < \pi$.

voltage across the inductor is negative, it is in such a direction as to forward bias the diode. The polarity of voltage across the inductor is as shown in Fig. 2.12 or 2.13.

When V_S changes from a positive to a negative value, there is current through the load at the instant $\omega t = \pi$ radians and the diode continues to conduct till the energy stored in the inductor becomes zero. After that the current tends to flow in the reverse direction and the diode blocks conduction. The entire applied voltage now appears across the diode.

Mathematical Analysis An expression for the current through the diode can be obtained as shown in the equations. It is assumed that the current flows for $0 < \omega t < \beta$, where $\beta > \pi$, when the diode conducts, the driving function for the differential equation is the sinusoidal function defining the source voltage. During the period defined by $\beta < \omega t < 2\pi$, the diode blocks current and acts as an open switch. For this period, there is no equation defining the behavior of the circuit. For $0 < \omega t < \beta$, Eq. (2.4) applies.

$$L\frac{di}{dt} + R \times i = E \times \sin(\theta), \text{ where } -0 \le \theta \le \beta \tag{2.4}$$

$$L\frac{di}{dt} + R \times i = 0 \tag{2.5}$$

$$\omega L\frac{di}{d\theta} + R \times i = 0 \tag{2.6}$$

$$i(\theta) = A \times e^{-R\theta/\omega L} \tag{2.7}$$

Given a linear differential equation, the solution is found out in two parts. The homogeneous equation is defined by Eq. (2.5). It is preferable to express the equation in terms of the angle θ instead of "t." Since $\theta = \omega t$, we get that $d\theta = \omega \cdot dt$. Then Eq. (2.5) gets converted to Eq. (2.6). Equation (2.7) is the solution to this homogeneous equation and is called the complementary integral.

The value of constant A in the complimentary solution is to be evaluated later. The particular solution is the steady-state response and Eq. (2.8) expresses the particular solution. The steady-state response is the current that would flow in steady state in a circuit that contains only the source, resistor, and inductor shown in the circuit, the only element missing being the diode. This response can be obtained using the differential equation or the Laplace transform or the ac sinusoidal circuit analysis. The total solution is the sum of both the complimentary and the particular solution and it is shown in Eq. (2.9). The value of A is obtained using the initial condition. Since the diode starts conducting at $\omega t = 0$ and the current starts building up from zero, $i(0) = 0$. The value of A is expressed by Eq. (2.10).

Once the value of A is known, the expression for current is known. After evaluating A, current can be evaluated at different values of ωt, starting from $\omega t = \pi$. As ωt increases, the current would keep decreasing. For some values of ωt, say β, the current would be zero. If $\omega t > \beta$, the current would evaluate to a negative value. Since the diode blocks current in the reverse direction, the diode stops conducting when ωt reaches. Then an expression for the average output voltage can be obtained. Since the average voltage across the inductor has to be zero, the average voltage across the resistor and average voltage at the cathode of the diode are the same. This average value can be obtained as shown in Eq. (2.11).

$$i(\theta) = \left(\frac{E}{Z}\right)\sin(\omega t - \alpha) \tag{2.8}$$

where

$$\alpha = a\tan\left(\frac{\omega l}{R}\right) \text{ and } \quad Z^2 = R^2 + \omega l^2$$

$$i(\theta) = A \times e^{(-R\theta/\omega L)} + \frac{E}{Z}\sin(\theta - \alpha) \tag{2.9}$$

$$A = \left(\frac{E}{Z}\right)\sin(\alpha) \tag{2.10}$$

Hence, the average output voltage:

$$V_{OAVG} = \frac{E}{2\pi}\int_0^{\beta} \sin\theta \cdot d\theta = \frac{E}{2\pi} \times [1 - \cos(\beta)] \tag{2.11}$$

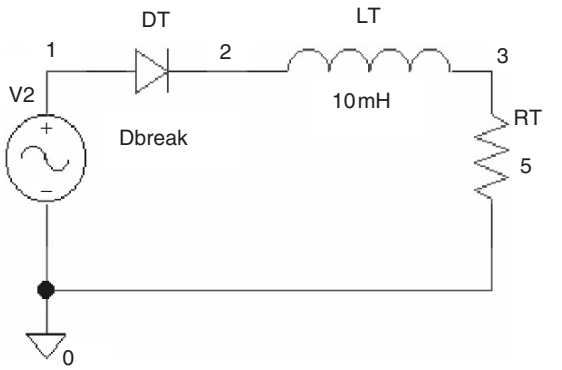

FIGURE 2.14 PSPICE model to study an R–L diode circuit.

PSPICE Simulation For simulation using PSPICE, the circuit used is shown in Fig. 2.14. Here the nodes are numbered. The ac source is connected between the nodes 1 and 0. The diode is connected between the nodes 1 and 2 and the inductor links the nodes 2 and 3. The resistor is connected from the node 3 to the reference node, that is, node 0. The circuit diagram is shown in Fig. 2.14.

The PSPICE program in textform is presented below.

```
*Half-wave Rectifier with RL Load
*An exercise to find the diode current
VIN 1 0 SIN(0 100 V 50 Hz)
D1 1 2 Dbreak
L1 2 3 10 mH
R1 3 0 5 Ohms
.MODEL Dbreak D(IS=10N N=1 BV=1200
   IBV=10E-3 VJ=0.6)
.TRAN 10 uS 100 mS 60 mS 100 uS
.PROBE
.OPTIONS (ABSTOL=1N RELTOL=.01 VNTOL=1MV)
.END
```

The diode is described using the MODEL statement. The TRAN statement simulates the transient operation for a period of 100 ms at an interval of 10 ms. The OPTIONS statement sets limits for tolerances. The output can be viewed on the screen because of the PROBE statement. A snapshot of various voltages/currents is shown in Fig. 2.15.

From Fig. 2.15, it is evident that the current lags the source voltage. This is a typical phenomenon in any inductive circuit and is associated with the energy storage property of the inductor. This property of the inductor causes the current to change slowly, governed by the time constant $\tau = \tan^{-1}(\omega l/R)$. Analytically, this is calculated by the expression in Eq. (2.8).

2.7 Typical Applications of Diodes

A. In rectification

Four diodes can be used to fully rectify an ac signal as shown in Fig. 2.16. Apart from other rectifier circuits, this topology does not require an input transformer. However, they are used for isolation and protection. The direction of the current is decided by two diodes conducting at any given time. The direction of the current through the load is always the same. This rectifier topology is known as the full bridge rectifier.

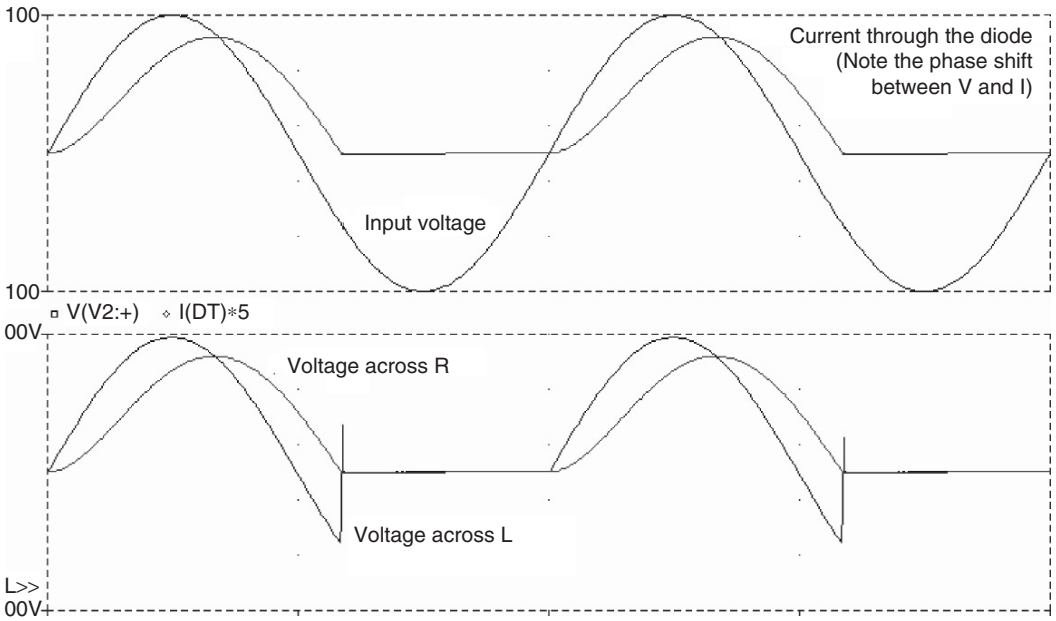

FIGURE 2.15 Voltage/current waveforms at various points in the circuit.

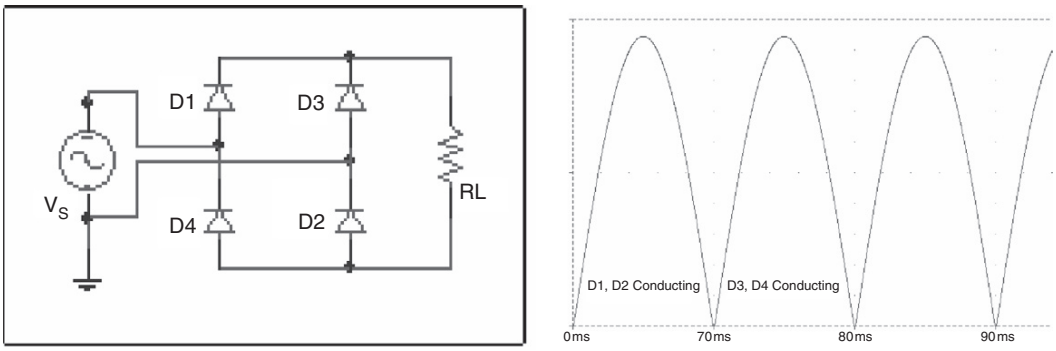

FIGURE 2.16 Full bridge rectifier and its output dc voltage.

The average rectifier output voltage:

$$V_{dc} = \frac{2V_m}{\pi}, \text{ where } V_m \text{ is the peak input voltage}$$

The rms rectifier output voltage:

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

This rectifier is twice as efficient as compared to a single phase one.

B. For voltage clamping

Figure 2.17 shows a voltage clamper. The negative pulse of the sinusoidal input voltage charges the capacitor to its maximum value in the direction shown. After charging, the capacitor cannot discharge, since it is open circuited by the diode. Hence the output voltage:

$$V_o = V_c + V_i = V_m(1 + \sin(\omega t))$$

The output voltage is clamped between zero and $2V_m$.

C. As voltage multiplier

Connecting diode in a predetermined manner, an ac signal can be doubled, tripled, and even quadrupled. This is shown in Fig. 2.18. As evident, the circuit will yield a dc voltage equal to $2V_m$. The capacitors are alternately charged to the maximum value of the input voltage.

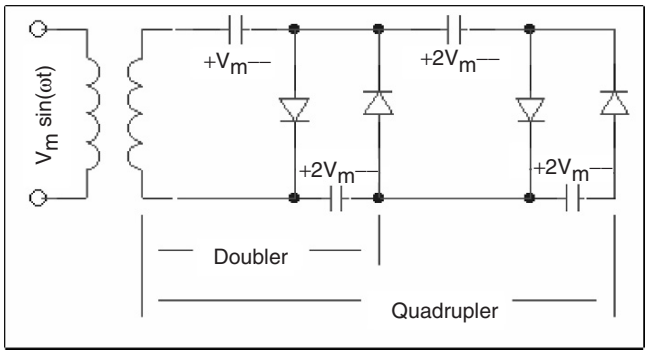

FIGURE 2.18 Voltage doubler and quadrupler circuit.

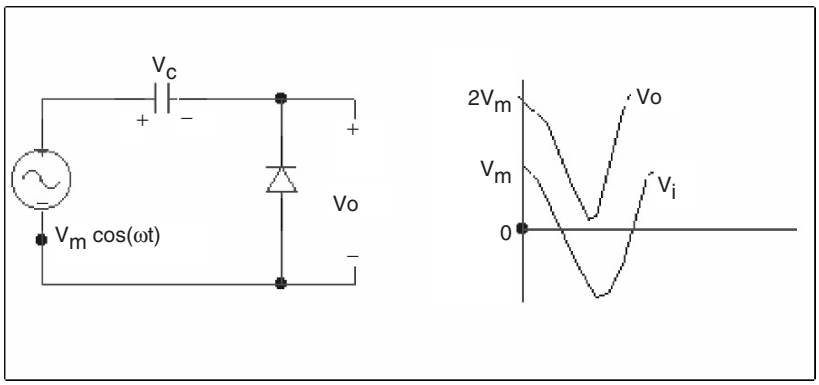

FIGURE 2.17 Voltage clamping with diode.

2.8 Standard Datasheet for Diode Selection

In order for a designer to select a diode switch for specific applications, the following tables and standard test results can be used. A power diode is primarily chosen based on forward current (I_F) and the peak inverse (V_{RRM}) voltage. For example, the designer chooses the diode type V30 from the table in Fig. 2.19 because it closely matches their calculated values of I_F and V_{RRM} without going over. However, if for some reason only the V_{RRM} matches but the calculated value of I_F comes higher, one should go for diode H14, and so on. Similar concept is used for V_{RRM}.

General-Use Rectifier Diodes

Glass Molded Diodes

$I_{F(AV)}$ (A)	V_{RRM}(V) / Type	50	100	200	300	400	500	600	800	1000	1300	1500
0.4	V30	-	-	-	-	-	-	-	yes	yes	yes	yes
1.0	H14	-	yes	yes	yes	yes	yes	yes	yes	yes	-	-
1.1	V06	-	-	yes	-	yes	-	yes	yes	-	-	-
1.3	___	-	-	yes	-	yes	-	yes	yes	-	-	-
2.5	U05	-	yes	yes	-	yes	-	yes	yes	-	-	-
3.0	U15	-	yes	yes	-	yes	-	yes	yes	-	-	-

FIGURE 2.19 Table of diode selection based on average forward current, $I_{F(AV)}$ and peak inverse voltage, V_{RRM} (courtesy of Hitachi semiconductors).

ABSOLUTE MAXIMUM RATINGS

Item	Type		V30J	V30L	V30M	V30N
Repetitive Peak Reverse Voltage	V_{RRM}	V	800	1000	1300	1500
Non-Repetitive Peak Reverse Voltage	V_{RSM}	V	1000	1300	1600	1800
Average Forward Current	$I_{F(AV)}$	A	0.4 (Single-phase half sine wave 180° conduction, TL = 100°C, Lead length = 10 mm)			
Surge(Non-Repetitive) Forward Current	I_{FSM}	A	30 (Without PIV, 10 ms conduction, Tj = 150°C start)			
I^2t Limit Value	I^2t	A^2s	3.6 (Time = 2 ~ 10 ms, I = RMS value)			
Operating Junction Temperature	T_j	°C	–50 ~ +150			
Storage Temperature	T_{s1g}	°C	–50 ~ +150			

Notes (1) Lead Mounting: Lead temperature 300°C max. to 3.2 mm from body for 5 sec. max.
(2) Mechanical strength: Bending 90° × 2 cycles or 180° × 1 cycle, Tensile 2kg, Twist 90° × l cycle.

CHARACTERISTICS (T_L=25°C)

Item	Symbols	Units	Min.	Typ.	Max.	Test Conditions
Peak Reverse Current	I_{RRM}	μA	–	0.6	10	All class Rated V_{RRM}
Peak Forward Voltage	V_{FM}	V	–	–	1.3	I_{FM}=0.4 Ap, Single-phase half sine wave 1 cycle
Reverse Recovery Time	t_{rr}	μs	–	3.0	–	I_F=2 mA, V_R=–15 V
Steady State Thermal Impedance	$R_{th(j-a)}$ / $R_{th(j-1)}$	°C/W	–	–	80 / 50	Lead length = 10 mm

FIGURE 2.20 Details of diode characteristics for diode *V30* selected from Fig. 2.19.

In addition to the above mentioned diode parameters, one should also calculate parameters like the peak forward voltage, reverse recovery time, case and junction temperatures, etc. and check them against the datasheet values. Some of these datasheet values are provided in Fig. 2.20 for the selected diode V30. Figures 2.21–2.23 give the standard experimental relationships between voltages, currents, power, and case temperatures for our selected V30 diode. These characteristics help a designer to understand the safe operating area for the diode, and to make a decision whether or not to use a snubber or a heat sink. If one is particularly interested in the actual reverse recovery time measurement, the circuit given in Fig. 2.24 can be constructed and experimented upon.

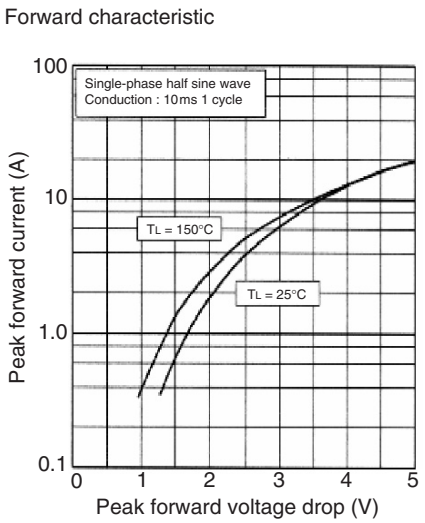

FIGURE 2.21 Variation of peak forward voltage drop with peak forward current.

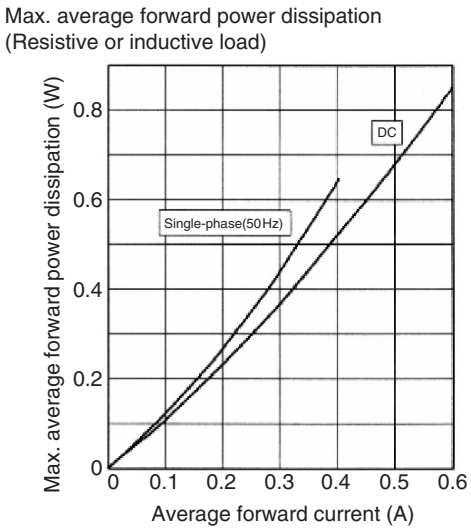

FIGURE 2.22 Variation of maximum forward power dissipation with average forward current.

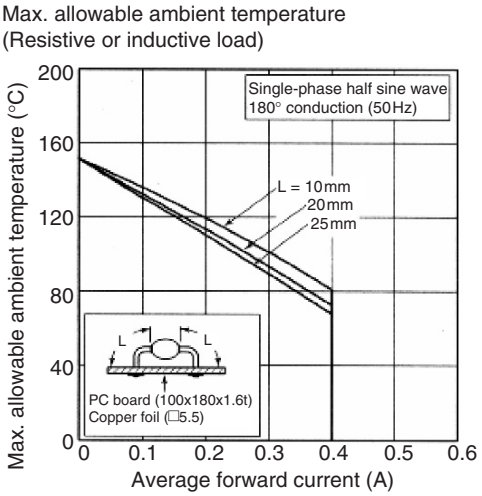

FIGURE 2.23 Maximum allowable case temperature with variation of average forward current.

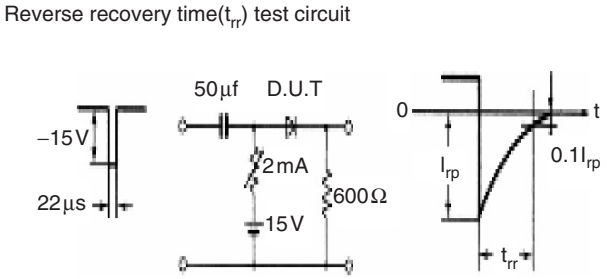

FIGURE 2.24 Reverse recovery time (t_{rr}) measurement.

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The Doherty Power Amplifier

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***Abstract*- In this contribution, the Doherty Power Amplifier (DPA) design concept is focused, discussing about different approaches to optimize its performance. For this purpose, the design, realization and measurement results of three prototypes working at 2.14GHz are presented. The first example is a Tuned Load DPA (TL-DPA) which shown an average drain efficiency of 40.7% with 3W of saturated output power in the obtained 6dB of OBO. The second DPA was designed implementing a Class F harmonic termination for the Main device allowing an improvement of roughly 15% in output power and efficiency levels with respect to the TL-DPA. The last DPA was realized using different bias voltages for the Main and Auxiliary amplifiers with the aim to increase the overall DPA gain.**

***Index Terms*- Doherty amplifier, GaN, Class F, Harmonic Tuning, LDMOS.**

I. INTRODUCTION

The Doherty Power Amplifier (DPA) architecture was introduced for the first time in 1936 by W. H. Doherty at the Bell Telephone Laboratories. It was the result of research activities devoted to find a solution to increase the efficiency of the first broadcasting transmitters, based on vacuum tubes [1]. In fact, being the signal to be transmitted amplitude modulated, its resulting Peak-to-Average Power Ratio (PAPR) critically affected the achievable average efficiency of traditional single-ended PAs [2]. The solution proposed by W. H. Doherty was based on the principle that lately was referred as "active load modulation" [3].
Nowadays, the problem related to the low average efficiency is still present due to the continuous increase in the complexity of modulation schemes, used to achieve higher and higher data rate transfer [4]. Therefore, when dealing with amplitude modulation signal, it is more useful to refer to the average efficiency rather than to the peak values. Clearly the average efficiency depends on both the PA instantaneous efficiency and the probability density function (PDF). Therefore, to obtain high average efficiency when time-varying envelope signals are used, the PA should work at the highest efficiency level in a wide range of its output (i.e. input) power. Since this requirement represents the main feature of the DPA architecture, it is being the preferred architecture for new communication systems [5-19].
In this contribution, the DPA concept will be reviewed in deep details showing different design approaches to improve its obtainable performance. A powerful theoretical treatment will be introduced with the aim to derive useful design guidelines for the PA designer.

II. DOHERTY IDEA & BENCHMARK

The modern DPAs are usually implemented by a proper combination of two active devices designed to operate as a Class AB (Main) and as a Class C (Auxiliary) power stages, respectively. The idea is to modulate the load seen by the Main device (vacuum tube in the original paper), in order to force the amplifier to operate in its maximum efficiency condition for a pre-determined range of input and/or output power levels. Such an action is performed by exploiting the active load modulation concept [3,5], by using the current supplied by the Auxiliary device into the external fixed load.

The typical DPA scheme is shown in Fig. 1, while the theoretical drain efficiency behavior of each device and DPA are depicted in Fig. 2.
Two operating regions are recognized:

- *A low power region*, where only the Main amplifier is active and the Auxiliary amplifier is kept off.
- *A medium power region* (referred as *Doherty region*) when both amplifiers are operating.

A third region, the saturation or peak power region, is referred when both amplifiers operate close to their respective saturation.
The range of the medium power region identifies the DPA output power back-off, OBO (and conversely the input power back-off, IBO) and can be controlled through a proper design choice [3,6].

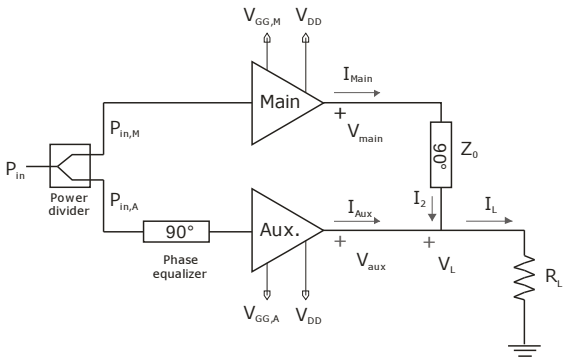

Fig. 1: Typical DPA configuration.

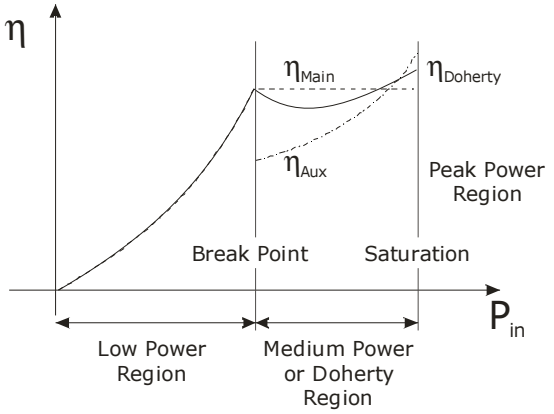

Fig. 2: Theoretical drain efficiency behaviour of DPA.

In the low power region, the Main device only is active, up to a saturation condition, represented by the output current $I_{critical}$ and with a dynamic load line (DLL) schematically depicted in Fig. 3 (dot load curve). When increasing the input power level, the Auxiliary device is automatically turned on, thanks to its Class C bias condition, supplying current in the external load (R_L). As a result, the load seen by the Main device is active modulated (i.e. it is reduced thanks to the output λ/4 transformer). In this way, the DLL of the Main device behaves as depicted in Fig. 3 (solid load curve), thus maintaining its efficiency almost constant at its maximum value in the entire *Doherty region* [3].

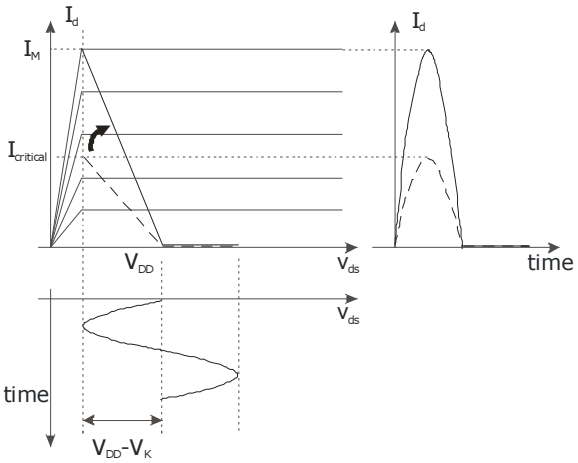

Fig. 3: DLL of the Main PA in the low power region.

Obviously, the phase difference introduced by the output λ/4 transformer (*λ/4 TL*), has to be properly compensated at the input, to constructively sum up the signals arising from both Main and Auxiliary devices. Such a compensation is usually performed by introducing a second *λ/4 TL* along the Auxiliary amplifier input path (see Fig. 1). The DPA scheme is completed by an uneven input power splitter. As it will be later demonstrated, the unequal power division between the Main and Auxiliary device inputs is essential to respect the following boundary conditions:

- when the Main device reaches the break point condition, the Auxiliary has to be turned on;
- afterwards, the Auxiliary device has to be driven into its conduction state to achieve the $I_{Max,Aux}$ value, while assuring that the Main device simultaneously reaches its maximum current $I_{Max,Main}$.

The Doherty technique is usually adopted to design PA for wireless systems and, in particular,

in base stations, working in L-S-C Band with time-varying envelope signals such as WiMax, UMTS, HSDPA, etc. In this field, a lot of experimental results have been published using different active device technologies such as Si LDMOS, GaN HEMT, GaAs PHEMT and GaAs HBT. Typically these DPA are realized in hybrid form and they work around 2.14 GHz with W-CDMA input signals. Drain efficiencies up to 70% have been demonstrated for output powers between 5W and 10W [10-13], whereas 50% of drain efficiency has been demonstrated for 250W output power [14]. Also for high frequency applications the DPA has been successfully implemented using GaAs MMIC technologies [9, 15, 16]. For instance, in [16] it has been reported a fully integrated DPA at millimeter-wave frequency band with 22dBm and 25% of output power and efficiency peak, respectively. Also DPA realizations based on CMOS technology was proposed [17-19]. However, in this case, due to the high losses related to the realization of required transmission lines, the performance achieved are quite low (peak efficiency lower than 15%).

III. BASIC DPA DESIGN GUIDELINES

In order to infer useful design relationships and guidelines, simplified models are assumed for the DPA elements. In particular, the passive components (*λ/4 TL* and power splitter) are assumed to be ideally lossless, while for the active device (in the following assumed as a FET type) an equivalent linearised model is assumed, as shown in Fig. 4. It is represented by a voltage-controlled current source, while for simplicity any parasitic feedback elements are neglected and all the other ones are embedded in the matching networks.

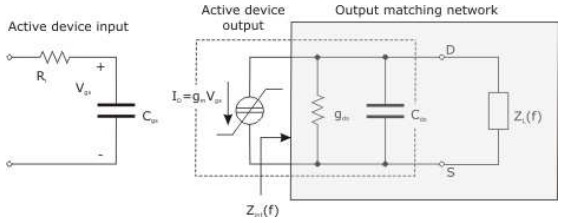

Fig. 4: Simplified model of the active device

The device output current source is described by a constant transconductance (g_m) in the saturation region, while an ON resistance (R_{ON}) is assumed for the ohmic region, resulting in the output I-V characteristics shown in Fig. 5.

In the DPA design, the device parameters to be considered are the maximum achievable output current (I_{Max}), the constant knee voltage (V_k) and the pinch-off voltage (V_p).

Usually, accounting for the PAPR of the system in which the DPA will be used, its design starts fixing the OBO value, defined as:

$$OBO = \frac{P_{out,DPA}\big|_{x=x_{break}}}{P_{out,DPA}\big|_{x=1}} = \frac{P_{out,Main}\big|_{x=x_{break}}}{P_{out,Main}\big|_{x=1} + P_{out,Aux}\big|_{x=1}} \qquad (1)$$

where the subscripts are used to refer to the entire DPA or to the single amplifiers (Main and Auxiliary respectively). Moreover, a parameter x ($0 \le x \le 1$) is used to identify the dynamic point in which those quantities are considered. In particular $x=0$ identifies the quiescent state, i.e. when no RF signal is applied to the input, while $x=1$ identifies the saturation condition, i.e. when the DPA reaches its maximum output power level. Similarly, $x=x_{break}$ identifies the break point condition, i.e. when the Auxiliary amplifier is turned on.

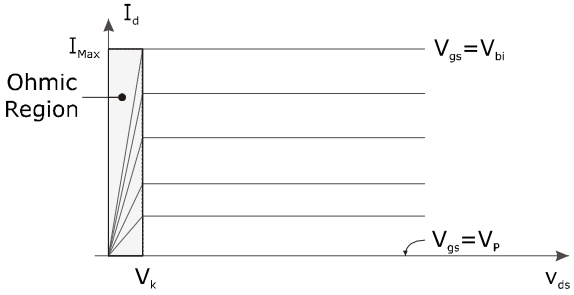

Fig. 5 I-V output characteristics of the simplified model.

Assuming a bias voltage V_{DD}, and assuming a Tuned Load configuration for both amplifiers, i.e. a short circuit loading condition for the impedances at harmonic frequencies, the following consideration can be done:

- The drain voltage amplitude of the Main device is equal to V_{DD}-V_k both for $x=x_{break}$ and $x=1$ as also highlighted by the load curve reported in Fig. 3.

- The same amplitude value is reached by the drain voltage of the Auxiliary device for *x=1*.

Consequently the output powers delivered by the Main and Auxiliary amplifiers in such peculiar conditions become:

$$P_{out,Main}\Big|_{x=x_{break}} = \frac{1}{2}\cdot(V_{DD}-V_k)\cdot I_{1,Main}\Big|_{x=x_{break}} \quad (2)$$

$$P_{out,Main}\Big|_{x=1} = \frac{1}{2}\cdot(V_{DD}-V_k)\cdot I_{1,Main}\Big|_{x=1} \quad (3)$$

$$P_{out,Aux}\Big|_{x=1} = \frac{1}{2}\cdot(V_{DD}-V_k)\cdot I_{1,Aux}\Big|_{x=1} \quad (4)$$

where the subscript "1" is added to the current in order to refer to its fundamental component.
Now, exploiting the constitutional equation of the output *λ/4 TL* and above all, remembering that the current on one side is a function of the voltage on the other side only (i.e. V_{DD}-V_k that is constant in the Doherty region), it is possible to write [3]:

$$V_L\Big|_{x=x_{break}} = (V_{DD}-V_k)\cdot\frac{I_{1,Main}\Big|_{x=x_{break}}}{I_{1,Main}\Big|_{x=1}} = \alpha\cdot(V_{DD}-V_k) \quad (5)$$

where α defines the ratio between the currents of the Main device at $x=x_{break}$ and *x=1*. Moreover, considering the matching network lossless, the voltage V_L is the one across R_L and its value at the saturation (*x=1*) has to be equal to V_{DD}-V_K. As a consequence, the following relationship rises:

$$\left.\frac{\alpha\cdot(V_{DD}-V_k)}{I_{1,Main(x=1)}}\right|_{x=x_{break}} = R_L = \left.\frac{(V_{DD}-V_k)}{I_{1,Main(x=1)}+I_{1,Aux(x=1)}}\right|_{x=1} \quad (6)$$

Therefore, from the previous equations it follows:

$$I_{1,Aux}\Big|_{x=1} = \frac{1-\alpha}{\alpha}\cdot I_{1,Main}\Big|_{x=1} \quad (7)$$

Finally, substituting (2)-(4) in (1) and accounting for (7), the following relationship can be derived:

$$OBO = \alpha^2 \quad (8)$$

which demonstrates that, selecting the desired OBO, the ratio between the Main device currents for $x=x_{break}$ and *x=1* is fixed by (5)as well as the ratio between the Main and Auxiliary fundamental current components as in (7).

Once again, since the DPA maximum output power value is usually fixed by the application requirements, it represents another constraint to be selected by the designer. Such maximum output power is reached for *x=1* and it can be estimated by the following relationship:

$$\begin{aligned} P_{out,DPA}\Big|_{x=1} &= \left(P_{out,Main}+P_{out,Aux}\right)\Big|_{x=1} \\ &= \frac{1}{\alpha}\cdot\frac{1}{2}\cdot(V_{DD}-V_k)\cdot I_{1,Main}\Big|_{x=1} \end{aligned} \quad (9)$$

which can be used to derive the maximum value of fundamental current component of Main device ($I_{1,Main|x=1}$), once its drain bias voltage (V_{DD}) and the device knee voltage (V_k) are fixed.
Finally, knowing the $I_{1,Main|x=1}$ value, it is possible to compute the values of R_L by (6) and the required characteristic impedance of the output *λ/4 TL* (Z_0) by using:

$$Z_0 = \frac{(V_{DD}-V_k)}{I_{1,Main}\Big|_{x=1}} \quad (10)$$

which is derived assuming that the output voltage (V_L) reaches the value V_{DD}-V_k for *x=1*.
Clearly the $I_{1,Main|x=1}$ value depends on the Main device maximum allowable output current I_{Max} and its selected bias point. The latter can be expressed as a percentage of the former through the following parameter:

$$\xi = \frac{I_{DC,Main}}{I_{Max,Main}} \quad (11)$$

being $I_{DC,Main}$ the quiescent (i.e. bias) current of the Main device. Consequently, *ξ=0.5* and *ξ=0* refer to a Class A and Class B bias condition respectively, while *0<ξ<0.5* identifies a generic Class AB bias condition.
Assuming a sinusoidal waveform for the drain current and performing a Fourier analysis it is easy to demonstrate that:

$$I_{1,Main}\Big|_{x=1} = \frac{I_{Max,Main}}{2\pi}\cdot\frac{\theta_{AB}-\sin(\theta_{AB})}{1-\cos\left(\frac{\theta_{AB}}{2}\right)} \quad (12)$$

being θ_{AB} the current conduction angle (CCA) of the Main output current, achieved for *x=1*. Moreover, the bias point *ξ* and the CCA θ_{AB} are related by the following relationship:

$$\theta_{AB} = 2\pi - 2\arccos\left(\frac{\xi}{1-\xi}\right) \quad (13)$$

Manipulating (12), the value of $I_{Max,Main}$, required to reach the desired maximum output power, can be estimated once the bias point ξ of the Main amplifier has been selected. In order to proper select the Main device bias point ξ reducing the AM/AM distortion, in [3] a figure of merit namely Gain Linear Factor (GLF) has been introduced. Fig. 6 shows the values of ξ, which theoretically assures the best GLF, as a function of the selected OBO. This design chart provides a guideline to select the proper ξ value, having fixed the desired OBO of the DPA.

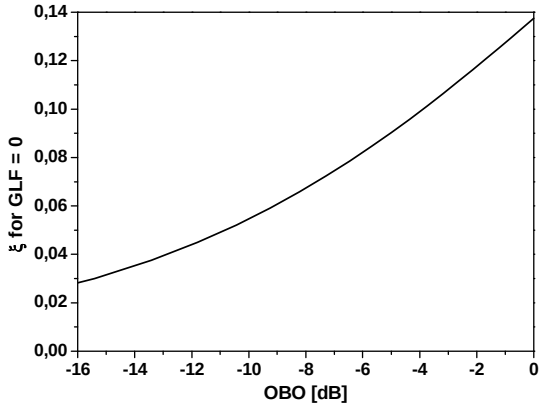

Fig. 6. Values of ξ assuring GLF=0, as function of the OBO.

The procedure followed to find the design parameters of the Main device can also be applied to determine the correspondent values of the Auxiliary one. In particular, it is possible to demonstrate that the final CCA of the Auxiliary device (θ_C) is a function of x_{break} value only [3]:

$$\theta_C = 2 \cdot \arccos\left(x_{break}\right) \quad (14)$$

Thus, once θ_C is known, the maximum current of the Auxiliary device ($I_{Max,Aux}$) can be easily calculated by using (12), replacing $\theta_{AB}=\theta_C$ and the subscript Main with Aux, since the value of $I_{1,Aux|x=1}$ should fulfill (7).

Moreover, to assure the right turning on condition of the Auxiliary amplifier, its output current has to become greater than zero at $x=x_{break}$. Consequently, to evaluate the x_{break} value, the following transcendental equation has to be numerically solved:

$$x_{break} \cdot \left[\theta_{Main} - \sin\left(\theta_{Main}\right)\right]\Big|_{x=x_{break}} = \alpha \cdot \left(\theta_{AB} - \sin\left(\theta_{AB}\right)\right) \quad (15)$$

It is obtained by replacing the Fourier expression of the fundamental current component of the Main device in the definition of the parameter α given by (5). As previously highlighted, the value of x_{break} is calculated once the OBO (i.e. α) and the Main device bias point (i.e. ξ) have been fixed.

To determine the Auxiliary device bias condition, a "virtual" bias current $I_{DC,Aux}$ can be defined, which represents the actual bias condition (gate voltage for FET devices) required to properly control its turning on condition. In particular, known the $I_{Max,Aux}$ and the corresponding CCA θ_C, the (negative) "virtual" bias current can be derived as follows:

$$I_{DC,Aux} = -I_{Max,Aux} \cdot \frac{x_{break}}{1 - x_{break}} \quad (16)$$

The latter has been inferred by imposing that the overall Auxiliary current is equal to zero at the break point.

Fig. 7 reports the behaviour of the ratio $I_{Max,Aux}/I_{Max,Main}$ as function of OBO and for different ξ values.

From the designer point of view, the maximum currents ratio can be used as an useful information to choice the proper device periphery or scaling factor.

In order to complete the DPA design, the input power splitter has to be dimensioned.

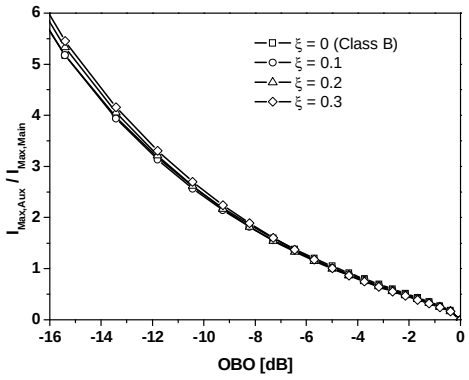

Fig. 7. Ratio between Auxiliary and Main maximum currents.

In Fig. 8 is reported the computed values for Λ_{Aux} (i.e. the amount of power delivered to the Auxiliary device with respect to the total input power), as function of OBO and ξ parameters, assuming for both devices the same values for g_m and R_{in} (i.e. device input impedance) [3].

Fig. 8 highlights that large amount of input power has to be provided to the Auxiliary device, requiring an uneven power splitting. This aspect dramatically affects the overall gain of the DPA, which typically becomes 5-6 dB lower if compared to the gain achievable by using a single amplifier only.

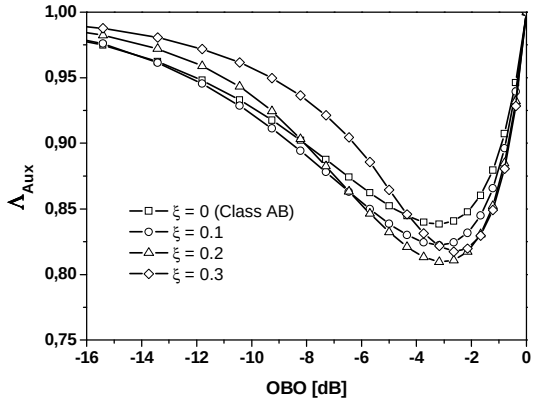

Fig. 8. Λ_{Aux} behavior as function of OBO and ξ.

Nevertheless, it has to remark that this largely unbalanced splitting factor has been inferred assuming a constant g_m for both devices. Such approximation is sufficiently accurate in the saturation region ($x=1$), while becomes unsatisfactory for low power operation (i.e. small signal). Thus, if the bias point of Main amplifier ξ is selected roughly lower than 0.2, the predicted gain overestimate the gain in actual experimental conditions.

Once the DPA design parameters have been settled, closed form equations for the estimation of the achievable performances can be obtained, as reported in [3].

An example of the inspected theoretical performance of a DPA designed to fulfill 6dB of OBO and 4W as maximum output power, are shown in Fig. 9.

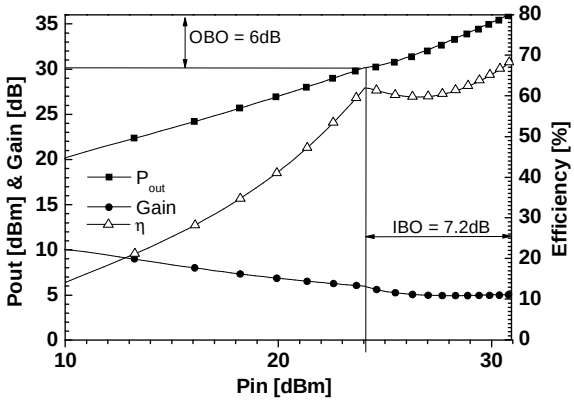

Fig. 9. Theoretical performances of a DPA.

Due to the different bias condition of both devices, the gain of the overall DPA shows a non constant behaviour, especially in the Doherty region. This results in a difference between the selected OBO and the input back-off (IBO), that generates an AM/AM distortion in the overall DPA. As already discuss, its value can be drastically reduced selecting the Main bias point following the GLF (Fig. 6).

In order to further clarify the DPA behaviour, Fig. 10 shows the fundamental drain currents and voltages for both Main and Auxiliary devices.

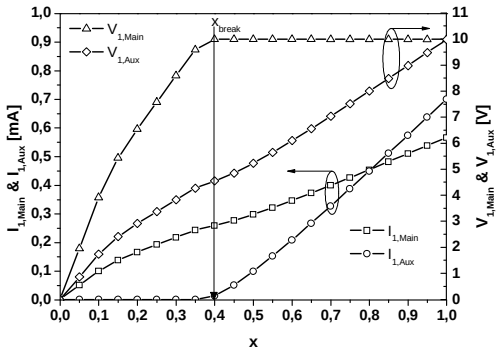

Fig. 10. Fundamental current and voltage components of Main and Auxiliary.

These behaviours can be used in the design flow to verify if the DPA operates in a correct way. In particular, the attention has to be focused on the Main voltage, which has to reach, at the break point (x_{break}), the maximum achievable amplitude (10V in this example) in order to maximize the efficiency. Moreover, the Auxiliary current can

be used to verify that the device is turned on at the right dynamic instant. Finally, the designer has to pay attention if the Auxiliary current reaches the expected value at the saturation (*x=1*), in order to perform the desired modulation of the Main resistance.

IV. ADVANCED DPA DESIGN GUIDELINES

In the previous section the basic DPA scheme based on Tuned Load configuration for both Main and Auxiliary amplifiers has been analyzed. Obviously, other solutions are available, still based on the load modulation principle, but developed with the aim to further improve the features of the DPA, by using some additional free design parameters. For instance, to improve the overall efficiency in a DPA configuration with respect to the simple Tuned Load one, high efficiency design strategies can be adopted in the synthesis of both Main and Auxiliary amplifiers [21]. However, due to the Class C bias condition for the Auxiliary device, the optimum solution for the latter is the classical Tuned Load one [21].

Conversely, for the Main amplifier, which is normally operating in a Class AB bias, the efficiency can be improved by using for instance Class F strategy [22]. Such design strategy implies that the second harmonic current component I_2 should be short circuited, while the fundamental (I_1) and the third one (I_3) should be terminated on impedance R_1 and R_3, respectively, to obtain a proper voltage harmonic component ratio [22]:

$$k_3 = \frac{V_3}{V_1} = \frac{R_3 \cdot I_3}{R_1 \cdot I_1} = 0.167 \tag{17}$$

Thus, in a Class F DPA (i.e. with Main amplifier in Class F configuration), the proper output harmonic loading conditions have to be fulfilled across the Main device, accounting for the load modulation effect in the medium power region.
In particular, it is possible to compute the theoretical load modulation required for the third harmonic, in order to fulfill (17) accounting for the modulation of R_1. In Fig. 11 is reported the ratio between the values required for R_3 at the end of the low power region ($x=x_{break}$) and at the end of the Doherty region, i.e. at saturation (x=1), as a function of the Main device bias point (ξ) and the selected OBO.
As it can be noted, the $R_{3,ratio}$ (i.e. the degree of modulation required for the third harmonic loading condition) increases with the bias point (ξ) and OBO values (α).
Nevertheless, the modulation of R_3 through the output λ/4 TL and the Auxiliary current, critically complicate the design and can be usually neglected if the Main device bias point is chosen nearly Class B condition, i.e. $\xi<0.1$, being $R_{3,ratio}\approx 1$. Under such assumption, it is possible to compute the Class F DPA design parameters as compared to the Tuned Load case. In particular, it is possible to demonstrate that the output load R_L and the Z_0 of the output *λ/4 TL* become:

$$R_{L,F} = \frac{R_{L,TL}}{1.15} \quad \& \quad Z_{0,F} = Z_{0,TL} \tag{18}$$

being $R_{L,TL}$ given by (6) and Z_0 by (10). Finally, regarding the power splitter dimensioning, it is required a different power splitting ratio, resulting in:

$$\Lambda_{Aux,F} = \frac{1.322 \cdot \Lambda_{Aux,TL}}{1 + 0.322 \cdot \Lambda_{Aux,TL}} > \Lambda_{Aux,TL}$$
$$\Lambda_{Main,F} = 1 - \Lambda_{Aux,F} < \Lambda_{Main,TL} \tag{19}$$

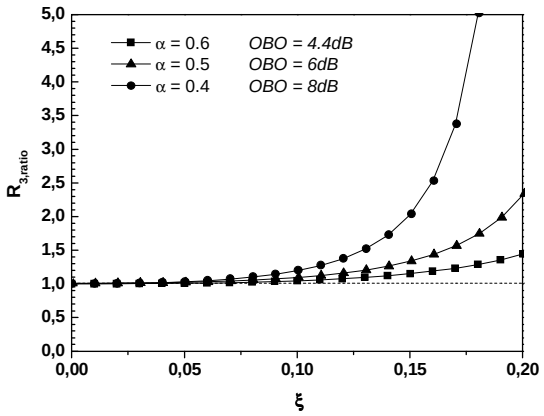

Fig. 11. $R_{3,ratio}$ as function of ξ for different OBO (α) values.

The expected behavior of the output current and voltage fundamental components for the Main

and the Auxiliary devices are reported in Fig. 12, assuming $\xi=0.082$ and $OBO=6dB$ (i.e. α=0.5).

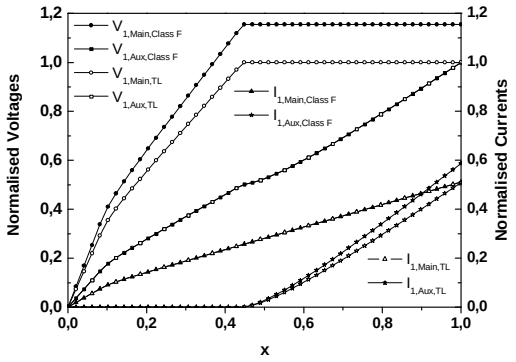

Fig. 12. Theoretical behavior of currents and voltages fundamental components, for Class F or TL design.

Similarly, in Fig. 13 are reported the comparisons in terms of output power and efficiency of Class F DPA with respect to Tuned Load DPA, normalized as a functions of the input signal *x*.

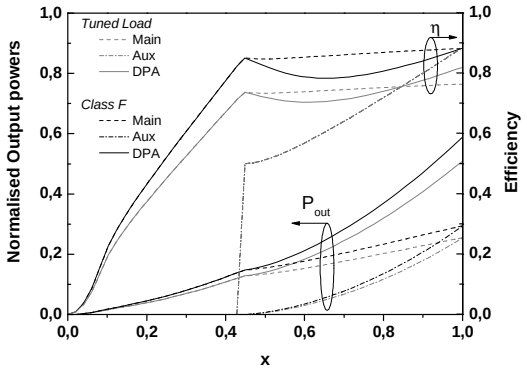

Fig. 13. Expected drain efficiency and output power behaviors for Class F and TL DPA.

Regarding the output performance of the DPA, it is to remark that the Class F DPA presents higher drain efficiency but lower gain as compared to the TL case. Now, in order to define a figure of merit to compare the two configurations, the following increasing factor $\Delta\eta_{add}$ has been defined:

$$\Delta\eta_{add}(\xi,\alpha,G_A)=\frac{\int_{x_{break}}^{1} PAE_{DPA,F}(\xi,\alpha,G_A,x)\,dx}{\int_{x_{break}}^{1} PAE_{DPA,TL}(\xi,\alpha,G_A,x)\,dx} \quad (20)$$

It represents the ratio between the PAE, integrated in the IBO, of the Class F and Tuned Load configuration. Therefore it is a function of the Main device bias point ξ, the output back-off selected α, and the gain in Class A of the chosen active devices (G_A). The contour lines of the $\Delta\eta_{add}$ as a function of α and G_A for $\xi=0.082$ (optimum bias point for linearity issue [3]), are reported in Fig. 14.

The $\Delta\eta_{add}$ indicates which configuration, between Class F and TL, is better to realise a DPA, once the G_A and α values have been chosen. For instance, if $\Delta\eta_{add}<1$ then the Tuned Load configuration is better than a Class F solution for the Main amplifier, while conversely when $\Delta\eta_{add}>1$ then the Class F DPA achieve higher PAE with respect the TL DPA.

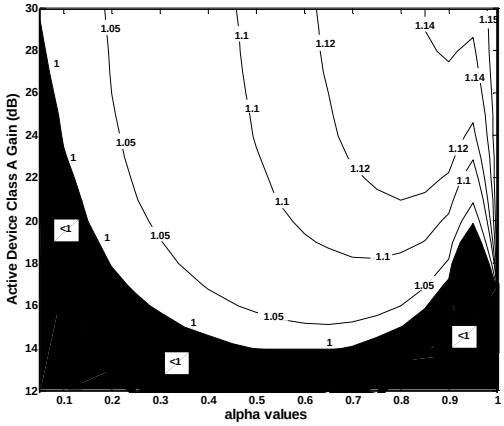

Fig. 14: Contour lines of $\Delta\eta_{add}$.

On the other hand, the adoption of different drain bias voltage for the two amplifiers (Main and Auxiliary) could be useful to increase the gain of the overall DPA [20]. In fact, in the DPA topology the voltage at the output common node, V_L in Fig. 1, at saturation is imposed by the Auxiliary drain bias voltage ($V_{DD,Aux}$) in order to fulfill the condition $V_L = V_{DD,Aux} - V_{k,Aux}$.

Thus, assuming a different bias, i.e. $V_{DD,Main}$ and $V_{DD,Aux}$ for the Main and Auxiliary devices respectively, and defining the parameter:

$$\beta=\frac{V_{DD,Main}-V_{k,Main}}{V_{DD,Aux}-V_{k,Aux}} \quad (21)$$

then the design relationships previously inferred have to be tailored accounting for different supplied voltages.

Therefore, the DPA elements R_L and Z_0 become:

$$R_L = \frac{\alpha^2}{\beta^2} \cdot R_{Main}\left(x_{break}\right) \tag{22}$$

$$Z_0 = \frac{V_{DD,Aux} - V_k}{I_{1,Main}\left(\theta_{AB}\right)} \tag{23}$$

Where:

$$R_{Main}\left(x_{break}\right) = 2\frac{V_{DD,Main} - V_{k,Main}}{I_{M,Main}} \cdot \frac{\pi}{\alpha} \cdot \frac{1-\cos\left(\frac{\theta_{AB}}{2}\right)}{\theta_{AB} - \sin\left(\theta_{AB}\right)} \tag{24}$$

Moreover, the Auxiliary and Main devices maximum output currents are now related through the following relationship:

$$I_{Max,Aux} = \beta \cdot I_{Max,Main} \cdot \frac{1-\alpha}{\alpha} \cdot \frac{1-\cos\left(\frac{\theta_C}{2}\right)}{\theta_C - \sin\left(\theta_C\right)} \cdot \frac{\theta_{AB} - \sin\left(\theta_{AB}\right)}{1-\cos\left(\frac{\theta_{AB}}{2}\right)} \tag{25}$$

Which, clearly, highlights that a suitable selection of the Auxiliary device supply voltage, i.e. $\beta<1$, could imply a lower maximum output current required from the Auxiliary device.

Conversely, the saturated output power of the Doherty (for $x=1$) is still related to both the Main device supplied voltage and its maximum output current, i.e.:

$$P_{out,DPA(x=1)} = \frac{1}{2}\left(V_{DD,Main} - V_k\right) \cdot \frac{I_{1,Main}\left(\theta_{AB}\right)}{\alpha} = \frac{1}{\alpha} \cdot P_{out,Main,Max} = \frac{1}{\alpha^2} \cdot P_{out,Main,break} \tag{26}$$

Thus being not affected by the different drain voltage supplied for the Auxiliary device.

V. EXPERIMENTAL RESULTS

In this section, the design and the realization of some DPAs implementing the above reported design solutions are presented. All circuits are realized in hybrid technology for UMTS applications (centre frequency 2.14 GHz) and are designed in order to obtain 6dB of OBO.

The first example has been designed following the basic DPA design guidelines, implementing a Tuned Load harmonic configuration for both devices. A photo of the realized circuit is reported in Fig. 15 [6].

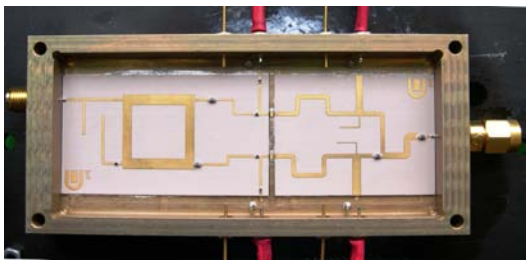

Fig. 15: Photo of the realized GaN TL-DPA.

In this case, the adopted active device, for both Main and Auxiliary amplifiers, is a GaN HEMT, 10x100µm gate fingers, 0.5µm gate length, resulting in 1mm of gate periphery.

The DPA was measured in Continuous Wave (CW) condition, fixing the drain voltage for both devices to $V_{DD}=15V$ and applying a gate voltage $V_{GG,Main}=-5.55V$ ($I_{DC,Main}=0.59mA$) and $V_{GG,Aux}=-15V$ for the Main and Auxiliary devices respectively. Fig. 16 shown the comparison between the measured and simulated performance.

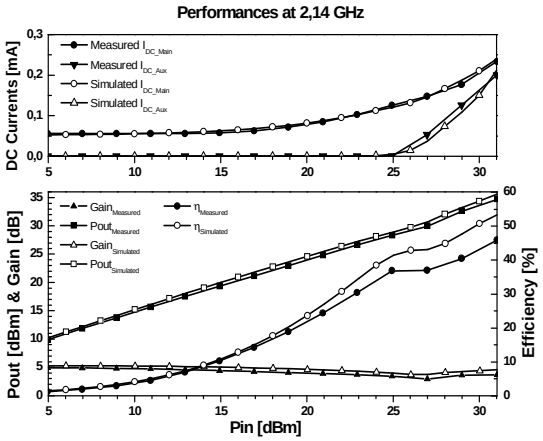

Fig. 16: TL-DPA performance.

In the obtained 6dB of OBO, an average drain efficiency of 40.7% is achieved with 3W of saturated output power.

The second DPA was designed implementing a Class F harmonic termination for the Main device (F-DPA), based on the same active devices (see Fig. 17).

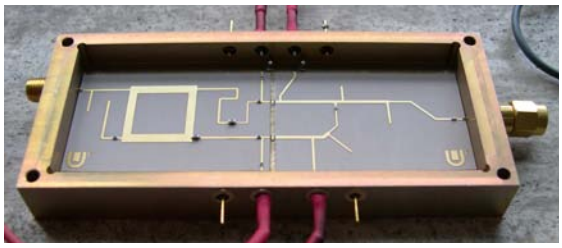

Fig. 17: Photo of the realized GaN Class F-DPA.

This approach was useful to highlight which are the differences in terms of design relationships and expected performances when a Tuned Load or Class F harmonic termination is used to built a DPA [23]. Such amplifier was measured in CW condition, fixing the drain voltage to $V_{DD}=15V$ and applying a gate voltage $V_{GG,Main}=-5.9V$ ($I_{DC,Main}=0.57mA$) and $V_{GG,Aux}=-11V$ for the Main and Auxiliary devices respectively.

The measured performances are reported in Fig. 18 compared with the simulated ones.

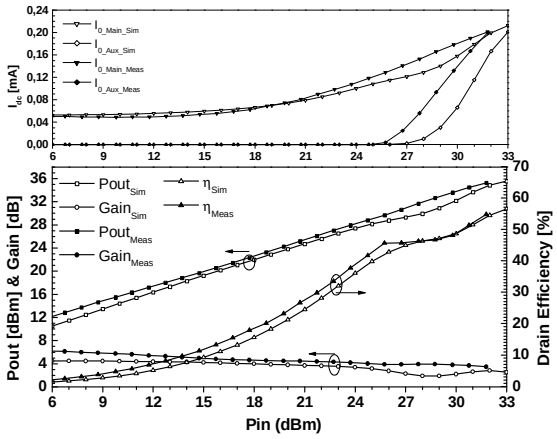

Fig. 18: Class F DPA performance.

As it can be seen, in the Doherty region an average drain efficiency of 50% has been registered, while achieving a saturated output power of 3.2W.

Moreover, Fig. 19 shows the comparison between the measured performances of the TL-DPA and the Class F-DPA as a function of the output power. As it can be noted, the Class F-DPA shows a drain efficiency roughly 15% higher than the efficiency of the TL-DPA, as expected after the Class F approach [22].

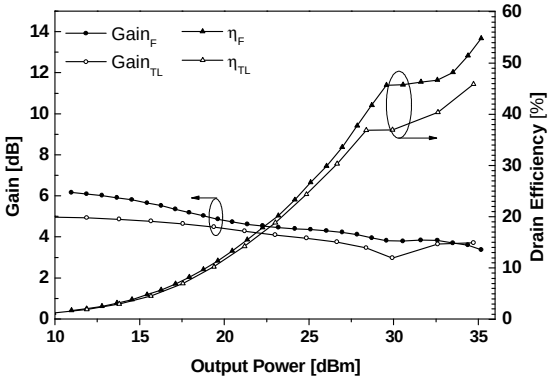

Fig. 19: TL-DPA vs. Class F-DPA.

The $\Delta\eta_{add}$ value coming from the results (1.05) is well in agreement with the expected one, as it can be noted from Fig. 14 considering the actual device Class A gain ($G_A=14.9dB$) and the desired OBO (0.501).

The last DPA here reported has been realized adopting different drain bias voltage for the two amplifiers (Main and Auxiliary), thus implementing the design guidelines developed to improve the overall DPA gain. In particular, to demonstrate the reliability of the proposed design methodology, two different DPAs have been designed and simulated, one with the same bias voltages for Main and Auxiliary devices (DPA_1), while the second one (DPA_2) by using different drain bias voltages, according to the guidelines reported in the previous section. For the design a LDMOS device provided by Freescale Semiconductor has been used, and the operating frequency of 2.14 GHz has been assumed

The DPA_1 has been designed by using as a drain voltage $V_{DD}=28V$, while for the Main device a quiescent bias current of 160 mA has been fixed as starting point.

For the DPA_2, initially the $V_{DD,Aux}$ was increased up to 35V, to maintain a safe margin with respect the breakdown limitation (70V). Then, to further reduce the splitting factor, also the drain voltage of the Main device ($V_{DD,Main}$) has been reduced, so increasing $I_{1,Main}$. The limit of such decreasing is related to the maximum output current which could be allowed for the Main device, that has

been assumed to be 2.5A, resulting in the voltage value $V_{DD,Main}=23.3V$.
For the input splitting a branch line has been adopted, thus including the phase compensation without adding a further quarter-wave line at the input. A photo of the realized DPA_2 is reported in Fig. 20.

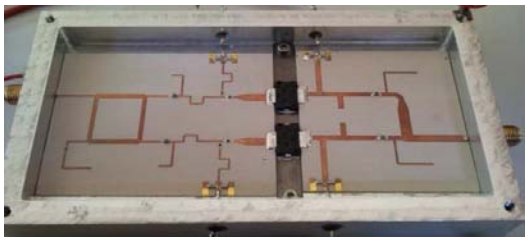

Fig. 20: Photo of the realised DPA.

The gain and the corresponding output power behaviours of the two designed DPAs are shown in Fig. 21, while in Fig. 22 is reported the drain efficiency behaviors.

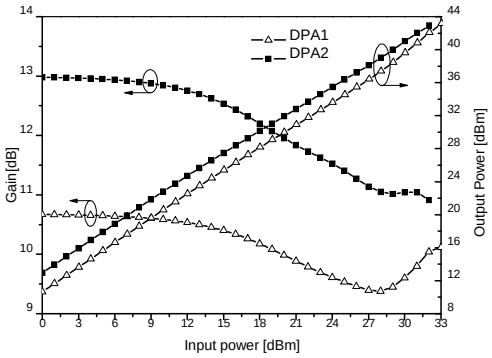

Fig. 21: Gain and Output Power of the two designed DPAs.

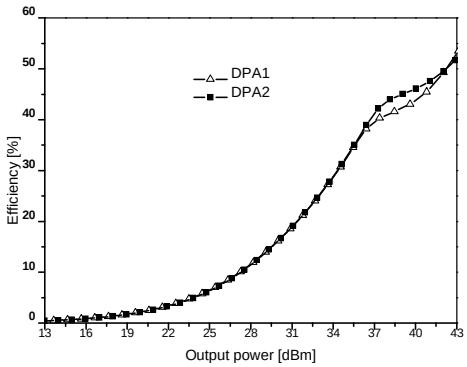

Fig. 22: Simulated efficiency of the two designed DPAs

As it can be noted from Fig. 22, both DPAs reach the same saturated output power level (43 dBm), with a quite similar efficiency behavior. However, from Fig. 21 it can be noted that an increase of roughly 2dB in power gain has been obtained with DPA_2. For both DPAs the efficiency is higher than 40% in 6dB of OBO.

VI. CONCLUSION

In this contribution, the Doherty Power Amplifier design concepts have been focused, extensively discussing about different approaches available to further optimize its performance. From the theoretical point of view, three different design approaches have been presented and validated through the realization of hybrid prototypes. In particular, the design, realization and measurement results of three prototypes working at 2.14GHz have been presented. The first example was a Tuned Load DPA which shown an average drain efficiency of 40.7% with 3W of saturated output power in the obtained 6dB of OBO. The second DPA was designed implementing a Class F harmonic termination for the Main device that allows an improvement of roughly 15% in output power and efficiency behavior with respect to the TL-DPA. The last DPA was realized using different bias voltages for the Main and Auxiliary amplifiers with the aim to increase the overall DPA gain. In this case, the reported results shown an increase of 2dB of gain with respect to a classical approach, maintaining almost the same output power and efficiency levels.

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